WE CLAIM:

1. A jitter measurement system comprising:

plural samplers for providing sample values, said plural samplers having respective signal inputs and strobe inputs;

a pulse source for generating a pulse;

circuitry coupling a signal to said signal inputs and said pulse source to said strobe inputs so that said samplers provide sample values corresponding to distinct transition points in said signal; and

a data processor for determining jitter associated with said signal in part as a function of said sample values.

2. The system of Claim 1, wherein said circuitry comprises at least one delay element connected to at least one delayed one of said plural samplers, said delay element being set to an amount less than the transition time of said signal, said samples being used to determine the jitter associated with a single zero-crossing of said signal.

3. The system of Claim 2, wherein said sample produced by said delayed sampler is used to determine the direction of a zero-crossing of said signal, said sample produced by a first one of said samplers being used to measure the time of said zero-crossing of said signal, the measured time of said zero-crossing and the direction of said zero-crossing being used by said data processor to calculate the jitter associated with said zero-crossing.

4. The system of Claim 3, wherein said data processor measures the time of said zero-crossing by extrapolating between said samples.

5. The system of Claim 1, wherein said circuitry comprises a delay element connected to one of said plural samplers, said delay element being set to an integer multiple of the bit period of said data signal, said samples being used to determine the time interval jitter associated with first and second zero-crossings of said signal.

6. A sampling apparatus capable of being used with high data rate signal jitter measurement systems, comprising:

a first sampling circuit connected to sample a data signal and output a first sample associated with a first value of said data signal;

a second sampling circuit connected to sample said data signal and output a second sample associated with a second value of said data signal, said second value being offset in time from said first value;

at least one sampling strobe connected to generate at least one output pulse to drive said first and second sampling circuits; and

a delay element connected to said second sampling circuit and configured to provide the offset in time between said first value and second value, said first and second samples being used to measure the jitter associated with said data signal.

7. The apparatus of Claim 6, further comprising:

a splitter connected to receive said data signal and provide said data signal to said first and second sampling circuits via respective first and second signal paths.

8. The apparatus of Claim 7, wherein said delay element is provided on said second signal path associated with said second sampling circuit, said first and second sampling circuits being further connected to receive said output pulse from said sampling strobe substantially simultaneously and output said first and second samples, respectively, substantially simultaneously.

9. The apparatus of Claim 6, wherein said delay element is provided on a path carrying said output pulse to said second sampling circuit, said delay element being configured to delay the sampling time of said data signal by said second sampling circuit as compared to the sampling time of said data signal by said first sampling circuit.

10. The apparatus of Claim 6, wherein said at least one sampling strobe comprises first and second sampling strobes associated with said first and second sampling circuits, respectively, and further comprising:

a single pattern trigger circuit connected to trigger said first and second sampling strobes at a time aligned with a first zero-crossing of said data signal, said delay element being operatively connected between said pattern trigger circuit and said second sampling circuit to delay triggering of said second sampling circuit at a time aligned with a second zero-crossing of said data signal, said first and second samples being used to determine the time interval jitter between said first and second zero-crossings.

11. The apparatus of Claim 6, wherein said delay element is set to an amount less than the transition time of said data signal, said second sample being used to determine the transition direction associated with a zero-crossing of said data signal in order to determine the jitter associated with said zero-crossing, said zero-crossing being determined from said first sample.

12. The apparatus of Claim 11, further comprising:

a third sampling circuit connected to sample said data signal and output a third sample associated with a third value of said data signal;

a first additional delay element connected to said second sampling circuit, said first additional delay element being set to an integer multiple of the bit period of said data signal, said first and third samples being used to determine the time interval jitter between first and second zero-crossings associated with said data signal, said first zero-crossing being determined from said first sample;

a fourth sampling circuit connected to sample said data signal and output a fourth sample associated with a fourth value of said data signal, said fourth value being offset in time from said third value; and

a second additional delay element connected to said fourth sampling circuit, said second additional delay element being set to a fraction of the transition time of said data signal, said fourth sample being used to determine the transition direction associated with said second zero-crossing of said data signal in order to determine the jitter associated with said second zero-crossing, said second zero-crossing being determined from said third sample.

13. The apparatus of Claim 6, wherein said delay element is set to an integer multiple of the bit period of said data signal, said first and second samples being used to determine the time interval jitter between two zero-crossings associated with said data signal, said two zero-crossings being determined from said respective first and second samples.

14. The apparatus of Claim 13, further comprising:

a third sampling circuit connected to receive a reference clock signal and sample said reference clock signal to produce a first reference clock sample, said first reference clock sample being used to determine the phase of said reference clock signal at the time at least said first sample of said data signal is taken.

15. The apparatus of Claim 14, further comprising:

a splitter connected to receive said reference clock signal and split said reference clock signal into first and second signal paths, said reference clock signal being filtered to be sinusoidal, said first signal path being connected to said third sampling circuit;

an additional delay connected on said second signal path, said additional delay being configured to delay said reference clock signal on said second signal path by around ninety degrees; and

a fourth sampling circuit connected to receive said delayed reference clock signal and sample said delayed reference clock signal to produce a second reference clock sample, said first and second reference clock samples being used to determine the phase of said reference clock signal at the time at least said first sample of said data signal is taken, the phase being used to determine the true time that at least said first sample of said data signal is taken.

16. The apparatus of Claim 15, wherein said splitter and additional delay element are provided within a ninety degree hybrid coupler.

17. The apparatus of Claim 15, further comprising:

at least one counter connected to receive said reference clock signal and configured to count the number of cycles of said reference clock signal; and

at least one latch connected to said counter and configured to latch the counted number of cycles at the time at least said first sample is taken.

18. The apparatus of Claim 17, wherein said at least one counter comprises first and second counters associated with said first and second sampling circuits, respectively, and said at least one latch comprises first and second latches associated with said first and second sampling circuits, respectively, the number of cycles latched within said first and second latches being used to determine the absolute time interval between the true times associated with said first and second samples of said data signal, the absolute time interval being used to determine the time interval jitter associated with said two zero-crossings of said data signal.

19. The apparatus of Claim 6, further comprising:

first and second analog-to-digital converters connected to receive said first and second samples, respectively, and output first and second digital samples, respectively.

20. A sampling apparatus capable of being used with a high data rate jitter measurement system, comprising:

a first sampling circuit connected to receive a data signal, sample said data signal and output a first sample associated with a first value of said data signal;

a second sampling circuit connected to receive said data signal, sample said data signal and output a second sample associated with a second value of said data signal, said second value being offset in time from said first value;

at least one sampling strobe connected to provide at least one output pulse to drive said first and second sampling circuits;

a single pattern trigger circuit connected to trigger said at least one sampling strobe to generate said at least one output pulse; and

a delay element connected to said second sampling circuit and being set to an integer multiple of the bit period of said data signal, said first and second samples being used to determine the time interval jitter associated with said first and second zero-crossings of said data signal.

21. The apparatus of Claim 20, wherein said at least one sampling strobe comprises first and second sampling strobes connected to said pattern trigger circuit and being associated with said first and second sampling circuits, respectively, said first and second sampling strobes being connected to provide said respective output pulses to drive said first and second sampling circuits, said delay element being operatively connected between said pattern trigger circuit and said second sampling strobe to delay said output pulse produced by said second sampling strobe.

22. The apparatus of Claim 21, further comprising:

a splitter associated with said first sampling circuit and connected to receive a reference clock signal and split said reference clock signal into first and second signal paths, said reference clock signal being filtered to be sinusoidal;

a first additional delay connected on said second signal path, said first additional delay being configured to delay said reference clock signal on said second signal path by around ninety degrees;

a third sampling circuit connected to receive said reference clock signal and sample said reference clock signal to produce a first reference clock sample; and

a fourth sampling circuit connected to receive said delayed reference clock signal and sample said delayed reference clock signal to produce a second reference clock sample, said first and second reference clock samples being used to determine the phase of said reference clock signal at the time at least said first sample of said data signal is taken, the phase being used to determine the true time that at least said first sample of data signal is taken.

23. The apparatus of Claim 22, further comprising:

an additional splitter associated with said second sampling circuit and connected to receive said reference clock signal and split said reference clock signal into third and fourth signal paths, said reference clock signal being filtered to be sinusoidal;

a second additional delay connected on said fourth signal path, said second additional delay being configured to delay said reference clock signal on said fourth signal path by around ninety degrees;

a fifth sampling circuit connected to receive said reference clock signal on said first signal path and sample said reference clock signal to produce a third reference clock sample; and

a sixth sampling circuit connected to receive said delayed reference clock signal on said fourth signal path and sample said delayed reference clock signal to produce a fourth reference clock sample, said third and fourth reference clock samples being used to determine the phase of said reference clock signal at the time said second sample of said data signal is taken, the phase calculated using said third and fourth reference clock samples being used to determine the true time that said second sample of data signal is taken.

24. The apparatus of Claim 23, further comprising:

a first counter connected to said splitter associated with said first sampling circuit and configured to count the number of cycles of said reference clock signal received at said first sampling circuit at the time said first sampling circuit is triggered;

a first latch connected to said first counter and configured to latch a first counted number of cycles at the time at least said first sample is taken;

a second counter connected to said additional splitter associated with said second sampling circuit and configured to count the number of cycles of said reference clock signal received at said second sampling circuit at the time said second sampling circuit is triggered; and

a second latch connected to said second counter and configured to latch a second counted number of cycles at the time at least said second sample is taken, said first and second counted number of cycles being used to determine the absolute time interval between the true times associated with said first and second samples of said data signal, the absolute time interval being used to determine the time interval jitter associated with said first and second zero-crossings of said data signal.

25. A method for determining the jitter associated with high data rate data signal, comprising:

generating at least one output pulse to drive first and second sampling circuits;

providing a delay element connected to said second sampling circuit;

sampling said data signal by said first sampling circuit to produce a first sample associated with a first value of said data signal; and

sampling said data signal by said second sampling circuit to produce a second sample associated with a second value of said data signal, said second value being offset in time from said first value, said first and second samples being used to measure the jitter associated with said data signal.

26. The method of Claim 25, further comprising:

splitting said data signal onto first and second signal paths, said first signal path being connected to said first sampling circuit and said second signal path being connected to said second sampling circuit.

27. The method of Claim 26, wherein said step of providing further comprises:

providing said delay element on said second signal path associated with said second sampling circuit, said first and second sampling circuits being further connected to receive said output pulse substantially simultaneously and produce said first and second samples, respectively, substantially simultaneously.

28. The method of Claim 25, wherein said step of providing further comprises:

providing said delay element on a path carrying said output pulse to said second sampling circuit, said delay element being configured to delay the sampling time of said data signal by said second sampling circuit as compared to the sampling time of said data signal by said first sampling circuit.

29. The method of Claim 25, wherein said step of generating further comprises:

generating first and second output pulses associated with said first and second sampling circuits, respectively, and further comprising the step of:

providing a single trigger to generate said first and second output pulses, said delay element delaying triggering of said second output pulse.

30. The method of Claim 25, wherein said step of providing further comprises:

setting said delay element to an amount less than the transition time of said data signal, said second sample being used to determine the transition direction associated with a zero-crossing of said data signal in order to determine the jitter associated with said zero-crossing, said zero-crossing being determined from said first sample.

31. The method of Claim 25, wherein said step of providing further comprises:

setting said delay element to an integer multiple of the bit period of said data signal, said first and second samples being used to determine the time interval jitter between two zero-crossings associated with said data signal, said two zero-crossings being determined from said respective first and second samples.

32. The method of Claim 31, further comprising:

sampling a reference clock signal to produce a first reference clock sample, said first reference clock sample being used to determine the phase of said reference clock signal at the time at least said first sample of said data signal is taken.

33. The method of Claim 32, further comprising:

splitting said reference clock signal into first and second signal paths, said reference clock signal being filtered to be sinusoidal, said first reference clock signal being associated with said first signal path;

providing an additional delay connected on said second signal path, said additional delay being configured to delay said reference clock signal on said second signal path by around ninety degrees;

sampling said delayed reference clock signal on said second signal path to produce a second reference clock sample, said first and second reference clock samples being used to determine the phase of said reference clock signal at the time at least said first sample of said data signal is taken, the phase being used to determine the true time that at least said first sample of data signal is taken.

34. The method of Claim 33, further comprising:

counting the number of cycles of said reference clock signal; and

latching the counted number of cycles at the time at least said first sample is taken.

35. The method of Claim 34, wherein said step of counting comprises:

counting a first number of cycles of said reference clock signal associated with said first sampling circuit; and

counting a second number of cycles of said reference clock signal associated with said second sampling circuit, and wherein said step of latching further comprises:

latching a first counted number of cycles at the time said first sample is taken; and

latching a second counted number of cycles at the time said second sample is taken, said first and second counted number of cycles being used to determine the absolute time interval between the true times associated with said first and second samples of said data signal, the absolute time interval being used to determine the time interval jitter associated with two zero-crossings of said data signal.